FUP1 Application Note **Ver : 1.2**

USB to Audio PCM Processor for VoIP Application Note

1.0 Introduction

The purpose of this application note is to provide specific design and layout guidelines to print circuit board with the FUP1 based system.

2.0 Design for Signal Integrity

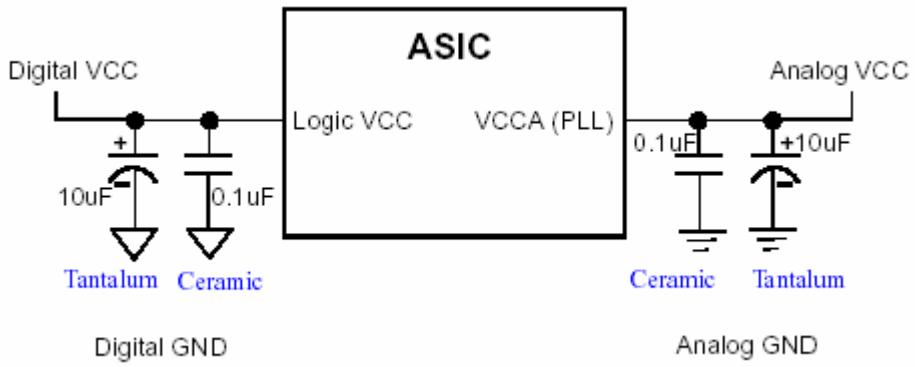
With the analog circuitry nature of the FUP1 data signals, careful attention must be paid to PCB layout and design to maintain adequate signal integrity.

2.1 FUP1 PLL application guidelines

a. Provide a tight tolerance on the VCCA voltage supply. A +/- 5% tolerance on VCCA is recommended.

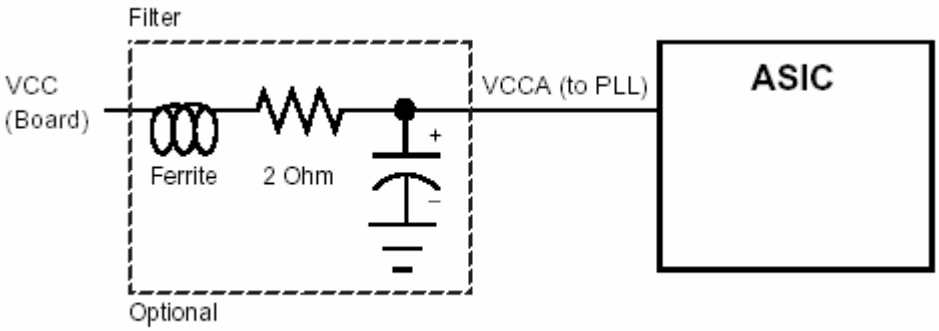
b. Provide a low-jitter XTAL1 signals. The maximum input jitter is +/- 150ps cycle-to-cycle. At higher magnitudes of input jitter, the output jitter will increase.

c. Minimum on-board VCC and ground noise by using adequate chip decoupling capacitors for high and low frequency noise. A minimum 0.1uF capacitors placed as close to each VCC pin as possible is recommended.
Minimize the length of trace between the ASIC power and the bypass capacitors pins.



d. Noise on VCC will cause phase jitter at the output of the PLL. To provide isolation from the noisy internal digital VCC signals, VCCA / GNDA is brought to a pair of dedicated package pins.

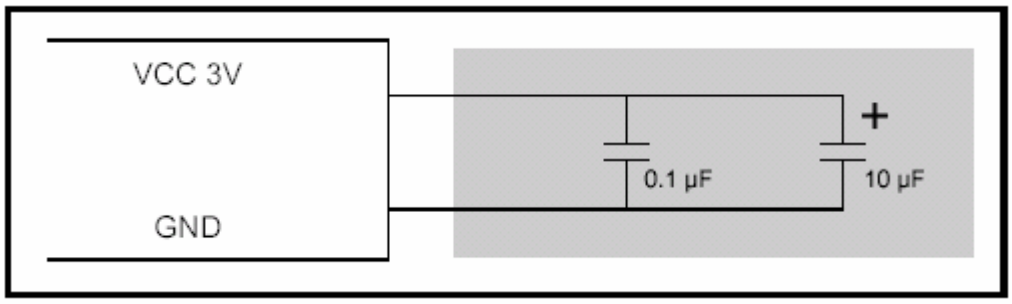
e. If little noise is expected at the board level, then VCCA can be connected directly to the digital VCC plane. In most circumstance, however, it is prudent to place a filter circuit on VCCA as shown below. All wire lengths should be kept as short as possible to minimize coupling from other signals.



2.2 FUP1 USB1.1 transceiver application guidelines

a. To provide isolation from the noisy internal digital VCC signals, VCCP / GNDP is brought to a pair of dedicated package pins.

b. The decoupling components should be connected closely to the power / ground pins outside the chip, as shown on below.



c. If little noise is expected at the board level, then VCCP can be connected directly to the digital VCC plane. In most circumstance, however, it is prudent to place a filter circuit on VCCP as shown on VCCA. All wire lengths should be kept as short as possible to minimize coupling from other signals.

d. For balance signals, the trace of D+ / D- to the USB connector should be kept short and symmetric.

e. FUP1 is a USB full-speed device, to configure the pull-up 1.5K ohm resistor outside the chip on D+ pin is needed.

3.0 System Clock

The FUP1 requires both of clock inputs are 12MHz and 2.048 (4.096) MHz.

In order to make sure the consecutive jitter range and paired JK / KJ jitter range can meet the specification of the USB spec. 1.1, we also suggest using Quartz Crystal instead of Ceramic Resonator in the 12MHz clock source.

4.0 Specific setting

4.1 Auxiliary Chip Select of Serial Peripheral Interface for the Caller ID module

a. To interface with the caller ID module, FUP1 (FUP1-D7F) support 4th SPI Chip Select to configure or write data to and read data from the caller ID module.

b. To enable the 4th SPI Chip Select, the alternate function of the GPIO3 pin for FUP1 (#63) or GPIO1 pin for FUP1-D7F (#26) must be first enable to act as /AUX_CS by setting the USB System Control Register, 0x01h, bit 7 to logic one for both FUP1 & FUP1-D7F.

c. Due to the FUP1 (FUP1-D7F) supports 4 mutual exclusive SPI bus, so the one and only one SPI can be activated at the same time through the USB System Control Register 0x01h as the following table.

Control Bits in the USB System Control Register			Selected CS Pin
SPI_SLIC_EN	SPI_DAA_EN	SPI_AUX_EN	
1	0	0	/SLIC_CS
0	1	0	/DAA_CS
0	0	0	EE_CS
0	0	1	/AUX_CS

4.2 EEPROM Types and Software Control

a. The FUP1 supports two types of EEPROM device, the SPI and I^2C, to store the product information such as the Vendor ID, Product ID and the Serial Number…,etc.

b. Both types support initial one time hardware access to the configured type of EEPROM that is setting through the EE_CS pin during the power-on configuration cycles to read those product information for the USB enumeration process.

c. Either the hardware or software control access to the EEPROM of I^2C type, the device SLA is always fixed on 1010000b.
d. For the software control access to the EEPROM of SPI type, the EE_Enable bit in SPI EEPROM Control Register 0x0Fh must be set to logic one.
e. For the software control access to the EEPROM of I^2C type, the SMB_RAM control bit in SMBus Control Register 0x09h must be set to logic zero, that is, only the one byte register addressing mode is supported.

5.0 Specific Control

5.1 SPI Control

a. All SPI control are full duplex, that is, the P_DOUT is receiving data during the P_DIN is transmitting the programmed data in the Serial Peripheral Interface Register 0x19h, 0x1Ah & 0x1Bh.
b. For 2 bytes SPI transfer operation, the receiving data can be always read by the Host from the Serial Peripheral Interface Second Data Register 0x1Ah once the Start_RW control bit in the Serial Peripheral Interface Control Register, 0x1Ch is transited from high to low.
c. For 3 bytes SPI transfer operation, the receiving data can be always read by the Host from the Serial Peripheral Interface Third Data Register 0x1Bh once the Start_RW control bit in the Serial Peripheral Interface Control Register, 0x1Ch is transited from high to low.

5.2 Interrupt Control

a. The FUP1 supports 4 external interrupt inputs and sampling the input status into the Interrupt Trigger Hold Register, 0x0Bh according the sampling mechanism that is controlled by the Interrupt Edge Trigger Register, 0x0Ch and Interrupt Edge / Level Selection Register, 0x0Dh.
b. The Interrupt Trigger Hold Register can be cleared through the Interrupt Trigger Reset Register, 0x0Eh by the Host. The Hold Register will not be cleared by itself.
c. If the interrupt sampling mechanism is setting to the level by the Interrupt Edge Trigger Register, 0x0Ch, then the external interrupt inputs will be sampled by the system clock (12MHz) into the Interrupt Trigger Hold Register, 0x0Bh.

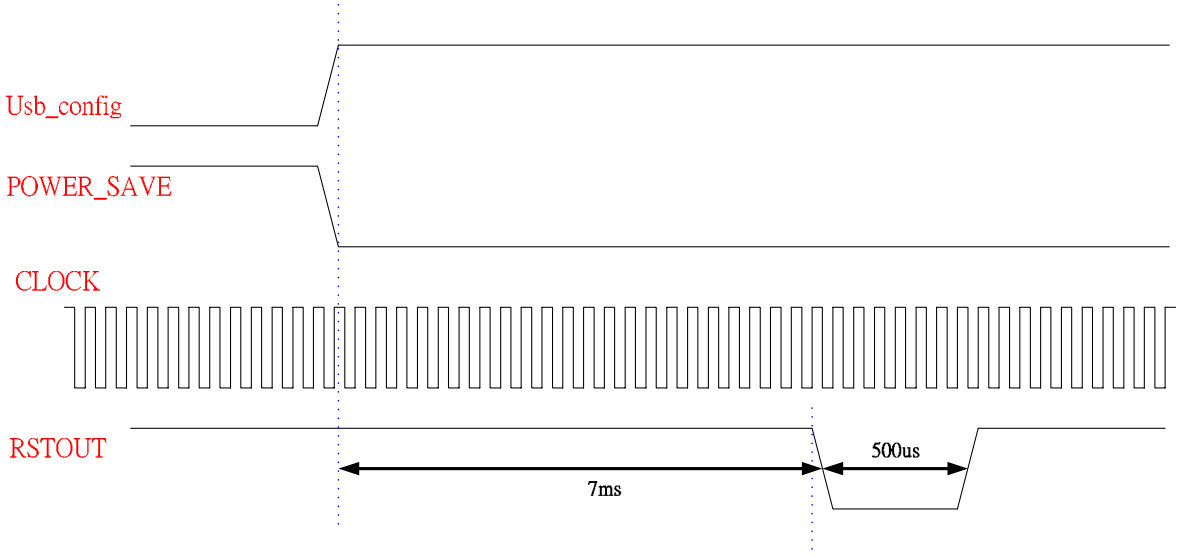
d. If the interrupt sampling mechanism is setting to the edge by the Interrupt Edge Trigger Register, 0x0Ch, only the transition edge on the external interrupt pins is meeting with the setting in the Interrupt Edge / Level Selection Register, 0x0Dh, then a correspond valid interrupt event will be set in the Interrupt Trigger Hold Register, 0x0Bh.

5.3 SMBus Control

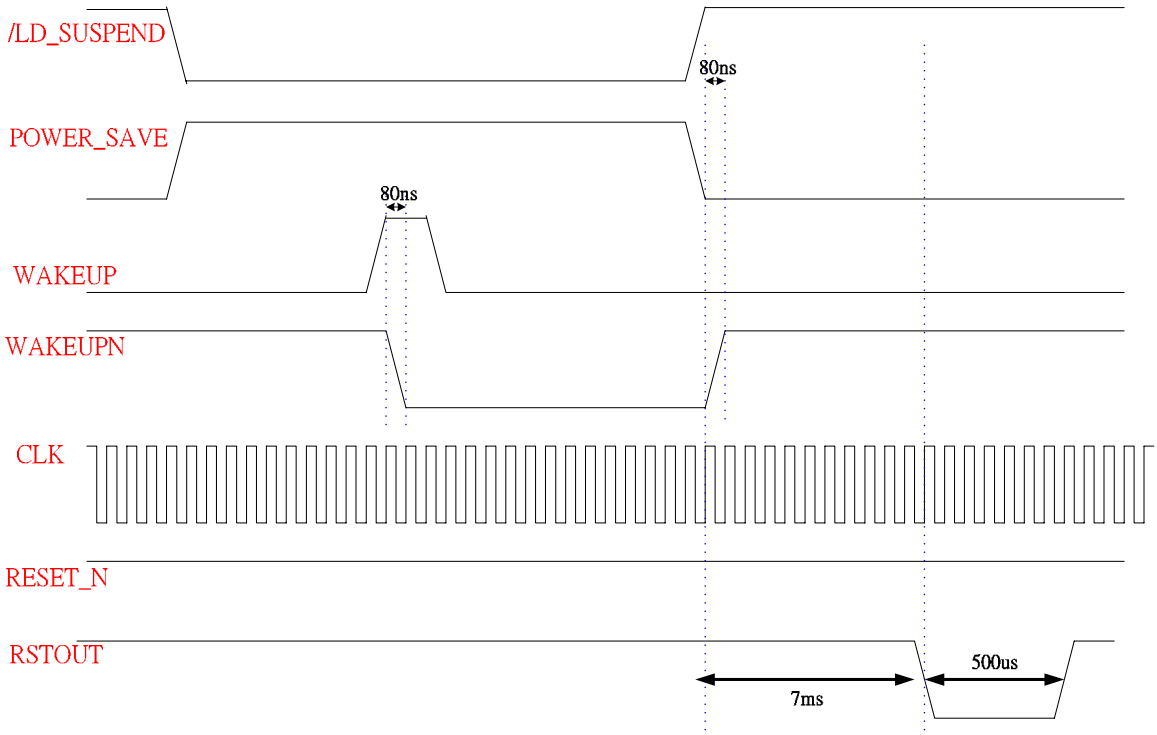
a. The FUP1 only supports the SMBus master transfer, that is, master read and master write, the slave transfer is not applicable.
b. For the SMBus master write, Host must program the SMBus Data Register, 0x02h ~ 0x07h to assemble the write transfer data, the SMBus Control Register, 0x08h to assign the SLA and transfer direction, the SMBus Control Register, 0x09h to decide the transfer rate and addressing mode, starting the transfer by setting the SMB_START bit to logic one for hardware transmitting, once the SMB_START bit is transited from high to low, then Host must read the SMB_OK bit to check if the SMBus master write transfer is successful or not.
c. For the SMBus master read, in addition to the SMBus Control Register 0x08h ~ 0x09h need to be programmed as the master write, the SMBus Data Register 0x02h must be programmed as the starting register address if the 1 byte register addressing mode is set, but an additional SMBus Data Register 0x03h also must be programmed as a part of the starting register address if the 2 bytes register addressing mode is set. The master read has the same staring and checking control as the master write, so only the SMB_OK bit in the SMBus Control Register, 0x09h is set as logic “1”, then the Host can get the SMBus read data from the SMBus Data Register, 0x02h ~ 0x07h.

5.4 Power Save Control

a. The FUP1 supports a power save control pin to save the device power as before the device is configured by the Host or the device is suspending.
b. Before the device is configured by the Host, the power save control pin is driven high to power down all peripheral components in the device except the FUP1 to keep the criteria of the minimum 100mA power consumption, and after the device is configured by the Host, the power save control pin is driven low to release the power done control, and waiting for about 7ms, the FUP1 will issue a RSTOUT about 500us to reset all peripheral components. The control sequence is as follow :



c. Once the FUP1 is suspending, the /LD_SUSPEND pin will be driven low to indicate this status, and the POWER_SAVE pin will be driven high to power down all peripheral components. Until a wakeup pulse is sensed on the WAKEUP pin or D+/D- pins are toggled by the Host, the POWER_SAVE is driven low to release the power down control, and again waiting for about 7ms, the FUP1 will issue a RSTOUT about 500us to reset all peripheral components. The control sequence is as follow :

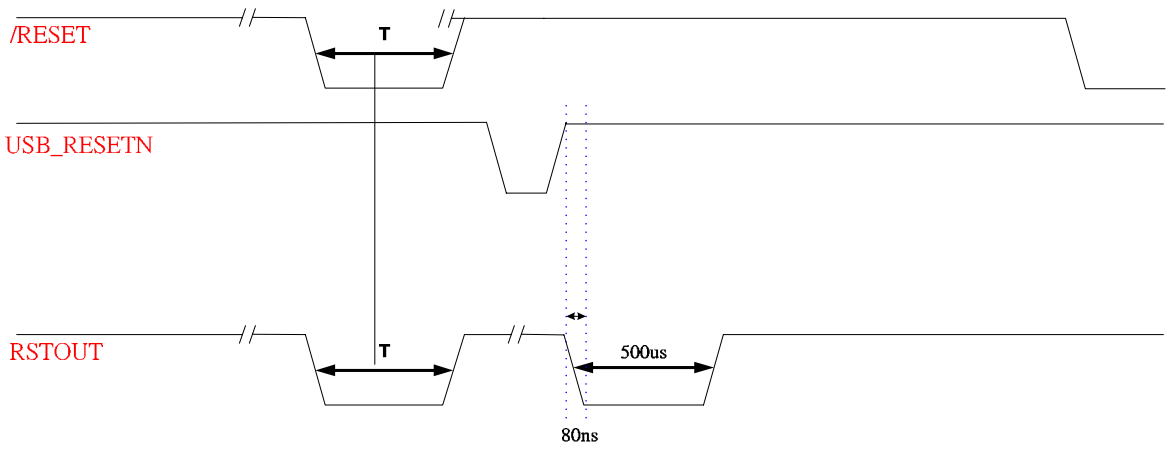


5.5 RSTOUT Control

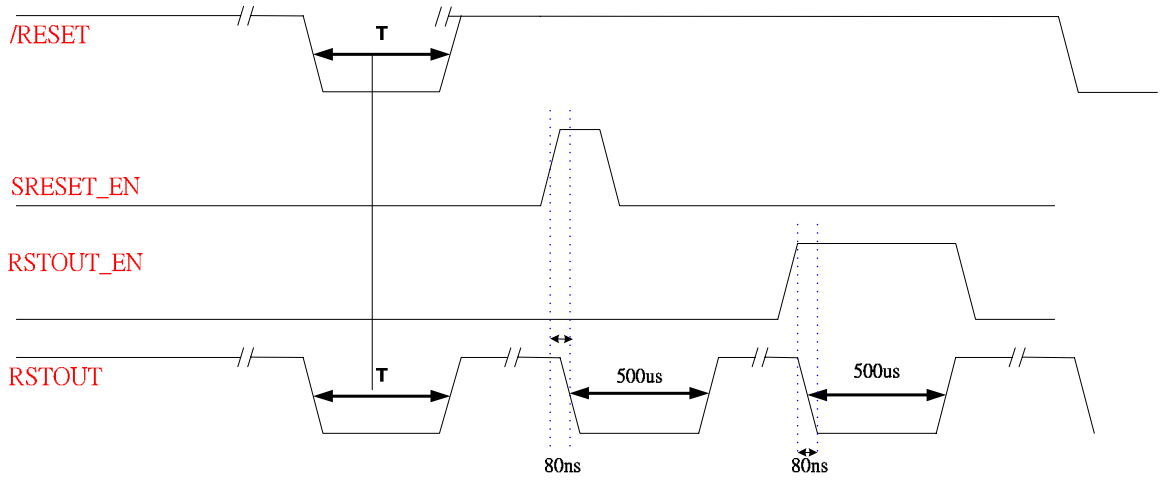
a. In addition to the Power Save Control to drive the RSTOUT pin, there are other driving control sources such as, /RESET input, USB Reset Command, Host Software Reset & Host RSTOUT control, and the driving polarity can be set by the Host through the USB System Control Register, 0x00h.

b. If the driving source of the RSTOUT is the /RESET input, then it's duty cycle is the same as the /RESET input, otherwise, it is a fix duty cycle of 500us.

c. The timing sequence for the RSTOUT that is driven by the USB Reset Command is as follow :



d. The timing sequence for other driving sources of the RSTOUT is as follow :

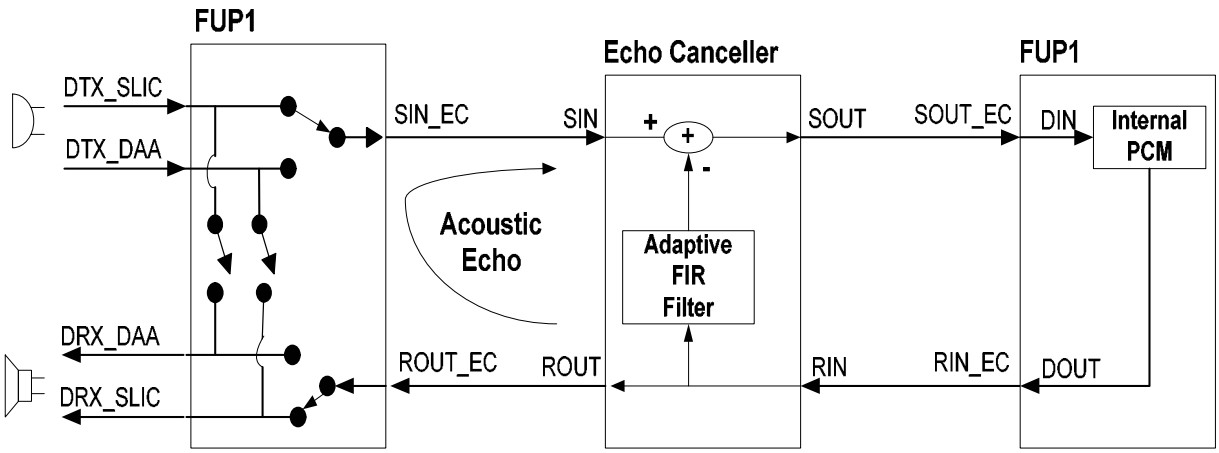


e. The SRESET_EN & RSTOUT_EN is setting by the USB System Control Register, 0x00h, and they are self-cleared after the end of the RSTOUT cycles.

6.0 Specific Connection

6.1 Echo Canceller Connection

a. The FUP1 is not built-in hardware echo canceller, so if the software echo canceller is not coding by the Host, then an external echo canceller is needed as the following connection.

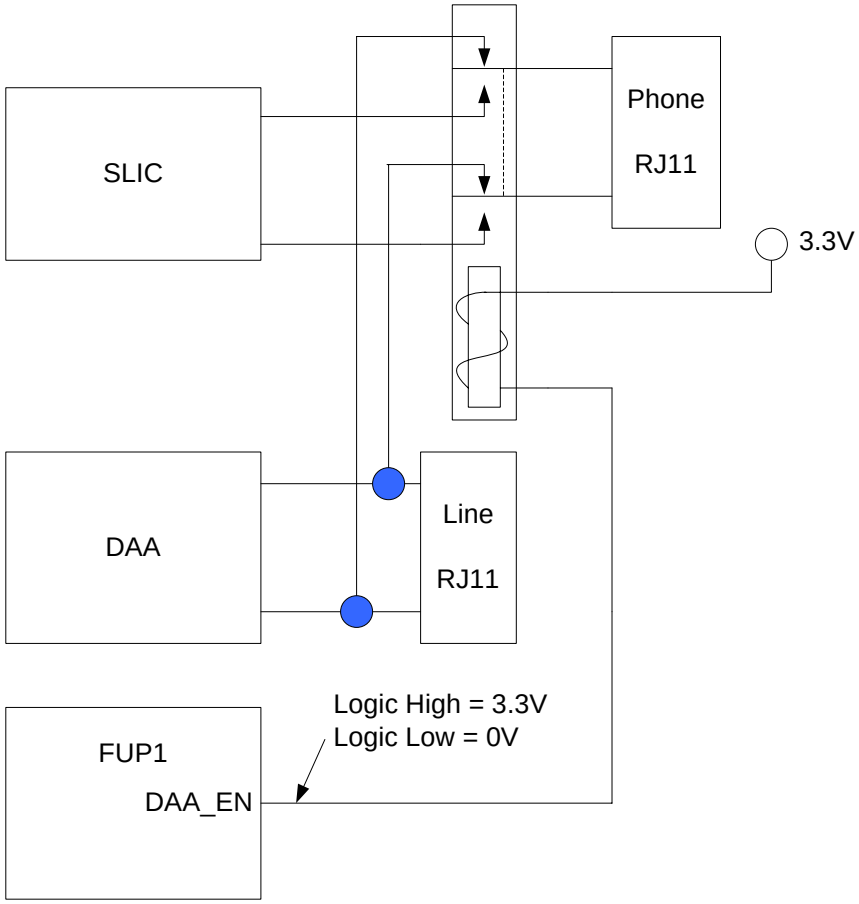


b. If an external echo canceller is connected, please note that if it not supports the PCM delay control, then both the SLIC / DAA and the FUP1 can't be programmed the PCM delay control by the Host, they must work without PCM delay.

c. The PCM Receive Start Delay Control value for DIN (SOUT_EC) and PCM Transmit Start Delay Control value for DOUT (RIN_EC) must be equal.

6.2 DAA / SLIC Switching Relay Connection

The FUP1 supports a high fan-out (max. 24 mA) control pin, DAA_EN (#10, for FUP1 & #2, for FUP1-D7F) to connect a external relay directly for switching between the DAA & SLIC as follow :



7.0 Revision History

Version	Date	Description
1.0	04/05/2005	Initial Release
1.1	09/30/2005	1. Add Content List 2. Revise 4.1c, to correct the SPI control table. 3. Add 4.2c,4.2e to add I^2C type of EEPROM. 4. Remove 4.3, the PID & VID Configuration. 5. Revise 5.2a,5.2d, the name of register 0x0Dh to meet the data sheet version 1.1. 6. Add 5.3, the SMBus Control. 7. Remove 6.2b, the optional external transistor to drive the DAA/SLIC switching relay.
1.2	10/06/2005	Change the FUP1-D to FUP1-D7F according Marketing Dept.'s naming rule conclusion.